

1. A test pattern generation and comparison apparatus in communication
with a built-in-self-test controller and functional integrated circuits ,
comprising:
a background and command decoder connected to receive test
background and command codes from said test controller, to
translate said test background and command codes to test stimulus
signals that, when applied to said functional integrated circuits,
create test response signals from said functional integrated circuits,
whereby said test stimulus signal has a plurality of bits; and
a plurality of latency buffers connected to said background and
command decoder to receive said test stimulus signals and to
adjust in time the relationship of said test stimulus signals as
required by said functional integrated circuits.
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- 15 2. The test pattern generation and comparison apparatus of claim 1 further
comprising:
a plurality of parallel-to-serial converters wherein each parallel-to-serial
converter is connected to one of the plurality of latency buffers, to
convert said test stimulus signals to a serialized test stimulus
signals to be scanned to a scan register of said functional
integrated circuit.
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3. The test pattern generation and comparison apparatus of claim 1 wherein
said background and command decoder comprises:
decode logic which decodes a high level command bus for activating
RAM control signals, and whereby the decode logic also controls
5 the transfer of the background pattern of expected results to the
error control module.
4. The test pattern generation and comparison apparatus of claim 1 wherein
said latency buffer comprises
10 a plurality of serially connected flip-flop circuits, whereby a first flip-flop
circuit of said plurality of serially connected flip-flop circuits has a
data input connected to said background and command decoder to
receive one bit of said test stimulus signal and an output connected
to a subsequent flip-flop circuit of the serially connected flip-flop
circuits, whereby each subsequent flip circuit of the serially
15 connected flip-flop circuits has an output connected to the input of a
following flip-flop circuit of said plurality of serially connected flip-
flop circuits, and whereby a last flip-flop circuit has an input
connected to an output of a previous flip-flop circuit and an output
20 containing a delayed bit of said test stimulus signal.
5. The test pattern generation and comparison apparatus of claim 4 whereby
the adjusting in time of the test stimulus signals is determined by a

number of flip-flop circuits in the plurality of serially connected flip-flop circuits and the number of latency buffers of the plurality of latency buffers is determined by a number of bits in the test stimulus signals and a period of a test access clocking signal.

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6. The test pattern generation and comparison apparatus of claim 5 wherein the number of flip-flop circuits is determined by the formula

$$N = \frac{\lambda}{\phi}$$

where:

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N is the number of said flip-flop circuits,

λ is the adjusting in time, and

ϕ is the period of the test access clocking signal.

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7. The test pattern generation and comparison apparatus of claim 2 wherein the parallel-to-serial circuit comprises:

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a first plurality of flip-flops whereby each flip-flop has a data input to receive one of a first portion of bits of said test stimulus signal and a clock input to receive a clocking signal to latch said the bit of the test stimulus signal;

a first plurality of multiplexor circuits whereby each multiplexor circuit has a first input to receive one of a remaining portion of bits of said test stimulus signal, second input to receive an output of one of the

first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

5 a second plurality of flip-flops, whereby each flip-flop of said plurality of
flip-flops has a data input connected to an output of one of the first
plurality of multiplexor circuits, and a clock input connected to
receive the clocking signal to latch the output of one of the first
plurality of multiplexor circuits to the output of said flip-flop of said
plurality of flip-flops; and

a second plurality of multiplexor circuits whereby each multiplexor circuit has a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

20 8. The test pattern generation and comparison apparatus of claim 1 further comprising:

a test response comparison circuit connected to said background and control decoder to receive an expected test response signal

providing a correct response expected from said integrated circuits in response to said test stimulus signals, and connected to said integrated circuit to receive a test response signal that is the response of the integrated circuit to said test stimulus signal.

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9. The test pattern generation and comparison apparatus of claim 8 wherein the test response comparison circuit comprises:

a comparator circuit to receive the test response signal and the expected test response signal, compare said test response signal to said expected test response signal and produce a test results signal indicating functioning of said integrated circuits.

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10. The test pattern generation and comparison apparatus of claim 9 wherein said comparator circuit comprises:

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An exclusive OR and OR logic tree which compares the RAM data output from the serial-to-parallel converter to an expected data output pattern from the background data.

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11. The test pattern generation and comparison apparatus of claim 9 wherein said test response comparison circuit further comprises:

a error-handling module to receive the test response signal and the expected test response signal and creates a diagnostic signal

indicating a location of any fault determined to exist within said integrated circuits.

12. The test pattern generation and comparison apparatus of claim 11

5 wherein said error handling module comprises:

a serial shift register composed of flip-flops, which are presettable from the serial-to-parallel data bus from the RAM and said shift register is loaded by the PASS/FAIL signal from the comparator, and whereby the serial output from the shift register transfers the data

10 for diagnosis.

13. The test pattern generation and comparison apparatus of claim 5 wherein

a hardware description of said test pattern generation and comparison apparatus requires the number of bits of the test stimulus signal and the adjusting in time of the test stimulus signal as parameters to automatically create a physical description of said test pattern generation and comparison apparatus during an automatic physical design of said integrated circuit for placement on said semiconductor substrate.

20 14. The test pattern generation and comparison apparatus of claim 1 wherein

said functional integrated circuits are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

15. A built-in-self test circuit incorporated with functional integrated circuits on a semiconductor substrate to verify correctness of operation of said functional integrated circuits, comprising:
- 5 a built-in-self-test controller to provide test background and command codes indicating tests to be performed on said function integrated circuits; and
- a test pattern generation and comparison apparatus in communication with the built-in-self-test controller to receive said test background and command codes and with said functional integrated circuits to transmit at least one test stimulus signal to said integrated circuit and to receive at least one test response signal to evaluate correctness of operation of said integrated circuit, comprising:
- 10 a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits, whereby said test stimulus signal has a plurality of bits; and
- 15 a plurality of latency buffers connected to said background and command decoder to receive said test stimulus signals and to adjust in time the relationship of said test stimulus signals as required by said functional integrated circuits.
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16. The built-in-self test circuit of claim 15 further comprising:
a plurality of parallel-to-serial converters wherein each parallel-to-serial
5 converter is connected to one of the plurality of latency buffers, to
convert said test stimulus to a serialized test stimulus signals to be
scanned to a scan register of said functional integrated circuit.
17. The built-in-self test circuit of claim 15 wherein said background and
10 command decoder comprises:
decode logic which decodes a high level command bus for activating
RAM control signals, and whereby the decode logic also controls
the transfer of the background pattern of expected results to the
error control module.
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18. The built-in-self test circuit of claim 15 wherein said latency buffer
comprises
a plurality of serially connected flip-flop circuits, whereby a first flip-flop
circuit of said plurality of serially connected flip-flop circuits has a
20 data input connected to said background and command decoder to
receive one bit of said test stimulus signal and an output connected
to a subsequent flip-flop circuit of the serially connected flip-flop
circuits, whereby each subsequent flip circuit of the serially

connected flip-flop circuits has an output connected to the input of a following flip-flop circuit of said plurality of serially connected flip-flop circuits, and whereby a last flip-flop circuit has an input connected to an output of a previous flip-flop circuit and an output containing a delayed bit of said test stimulus signal.

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19. The built-in-self test circuit of claim 18 whereby the adjusting in time of the test stimulus signals is determined by a number of flip-flop circuits in the plurality of serially connected flip-flop circuits and the number of latency

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buffers of the plurality of latency buffers is determined by a number of bits in the test stimulus signals.

20. The built-in-self test circuit of claim 19 wherein the number of flip-flop circuits is determined by the formula:

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$$N = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

λ is the adjusting in time, and

ϕ is the period of the test access clocking

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signal.

21. The built-in-self test circuit of claim 16 wherein the parallel-to-serial circuit comprises:

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a first plurality of flip-flops whereby each flip-flop has a data input to receive one of a first portion of bits of said test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the test stimulus signal;

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a first plurality of multiplexor circuits whereby each multiplexor circuit has a first input to receive one of a remaining portion of bits of said test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

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a second plurality of flip-flops, whereby each flip-flop of said plurality of flip-flops has a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the output of one of the first plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and

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a second plurality of multiplexor circuits whereby each multiplexor circuit has a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of

said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

- 5 22. The built-in-self test circuit of claim 15 further comprising:
a test response comparison circuit connected to said background and
control decoder to receive an expected test response signal
providing a correct response expected from said integrated circuits
in response to said test stimulus signals, and connected to said
integrated circuit to receive a test response signal that is the
response of the integrated circuit to said test stimulus signal.

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23. The built-in-self test circuit of claim 22 wherein the test response
comparison circuit comprises:
a comparator circuit to receive the test response signal and the
expected test response signal, compare said test response signal
to said expected test response signal and produce a test results
signal indicating functioning of said integrated circuits.

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20 24. The built-in-self test circuit of claim 23 wherein said comparator circuit
comprises:

an exclusive OR and OR logic tree which compares the RAM data output from the serial-to-parallel converter to an expected data output pattern from the background data.

- 5 25. The built-in-self test circuit of claim 22 wherein said test response comparison circuit further comprises:

a error-handling module to receive the test response signal and the expected test response signal and creates a diagnostic signal indicating a location of any fault determined to exist within said integrated circuits.

- 10 26. The built-in-self test circuit of claim 25 wherein said error handling module comprises:

a serial shift register composed of flip-flops, which are presettable from the serial-to-parallel data bus from the RAM and said shift register is loaded by the PASS/FAIL signal from the comparator, and whereby the serial output from the shift register transfers the data for diagnosis.

- 15 27. The built-in-self test circuit of claim 20 wherein a hardware description of said built-in-self test circuit requires the number of bits of the test stimulus signal and the adjusting in time of the test stimulus signal as parameters to automatically create a physical description of said built-in-self test circuit

during an automatic physical design of said integrated circuit for placement on said semiconductor substrate.

28. The built-in-self test circuit of claim 15 wherein said functional integrated circuits are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

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29. A computer implemented hardware description coding providing a description of a computer implemented hardware description coding to automatically create a physical description of said computer implemented hardware description coding during an automatic physical design of said integrated circuit for placement on said semiconductor substrate, whereby said computer implemented hardware description coding comprises:

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a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits, whereby said test stimulus signal has a plurality of bits; and

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said test stimulus

signals and to adjust in time the relationship of said test stimulus signals as required by said functional integrated circuits.

- 5 30. The computer implemented hardware description coding of claim 29
further comprising:
- a descriptive coding of a plurality of parallel-to-serial converters
wherein each parallel-to-serial converter is connected to one of the
plurality of latency buffers, to convert said test stimulus to a
10 serialized test stimulus signals to be scanned to a scan register of
said functional integrated circuit.
31. The computer implemented hardware description coding of claim 29
wherein said descriptive coding of background and command decoder
15 comprises:
- descriptive coding of decode logic which decodes a high level
command bus for activating RAM control signals, and whereby the
decode logic also controls the transfer of the background pattern of
expected results to the error control module.

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32. The computer implemented hardware description coding of claim 29
wherein said a descriptive coding of latency buffer comprises

a descriptive coding of a plurality of serially connected flip-flop circuits,
whereby a first flip-flop circuit of said plurality of serially connected
flip-flop circuits has a data input connected to said background and
command decoder to receive one bit of said test stimulus signal
5 and an output connected to a subsequent flip-flop circuit of the
serially connected flip-flop circuits, whereby each subsequent flip
circuit of the serially connected flip-flop circuits has an output
connected to the input of a following flip-flop circuit of said plurality
of serially connected flip-flop circuits, and whereby a last flip-flop
10 circuit has an input connected to an output of a previous flip-flop
circuit and an output containing a delayed bit of said test stimulus
signal.

33. The computer implemented hardware description coding of claim 32
15 whereby the adjusting in time of the test stimulus signals is determined by
a number of flip-flop circuits in the plurality of serially connected flip-flop
circuits and the number of latency buffers of the plurality of latency buffers
is determined by a number of bits in the test stimulus signals.

- 20 34. The computer implemented hardware description coding of claim 33
wherein the number of flip-flop circuits is determined by the formula:

$$N = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

λ is the adjusting in time, and

ϕ is the period of the test access clocking signal.

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35. The computer implemented hardware description coding of claim 30 wherein the parallel-to-serial circuit comprises:

a descriptive coding of a first plurality of flip-flops whereby each flip-flop has a data input to receive one of a first portion of bits of said test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the test stimulus signal;

a descriptive coding of a first plurality of multiplexor circuits whereby each multiplexor circuit has a first input to receive one of a remaining portion of bits of said test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

a descriptive coding of a second plurality of flip-flops, whereby each flip-flop of said plurality of flip-flops has a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the

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output of one of the first plurality of multiplexor circuits to the output
of said flip-flop of said plurality of flip-flops; and
a descriptive coding of a second plurality of multiplexor circuits
whereby each multiplexor circuit has a first input connected to a
first flip-flop of the plurality of flip-flops, second input connected to a
second flip-flop of the second plurality of flip-flops, and a select
input connected to the clocking signal to alternately transfer the first
input to an output of said multiplexor circuits and the second input
to the output, as said clocking signal changes from a first level to a
second level and from the second level to the first level.

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36. The computer implemented hardware description coding of claim 29
further comprising:
a descriptive coding of a test response comparison circuit connected to
said background and control decoder to receive an expected test
response signal providing a correct response expected from said
integrated circuits in response to said test stimulus signals, and
connected to said integrated circuit to receive a test response
signal that is the response of the integrated circuit to said test
stimulus signal.

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37. The computer implemented hardware description coding of claim 36
wherein the descriptive coding of the test response comparison circuit
comprises:
a descriptive coding of a comparator circuit to receive the test
response signal and the expected test response signal, compare
said test response signal to said expected test response signal and
produce a test results signal indicating functioning of said
integrated circuits.
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- 10 38. The computer implemented hardware description coding of claim 37
wherein said descriptive coding of comparator circuit comprises:
descriptive coding of an exclusive OR and OR logic tree which
compares the RAM data output from the serial-to-parallel converter
to an expected data output pattern from the background data.
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- 15 39. The computer implemented hardware description coding of claim 37
wherein said descriptive coding of test response comparison circuit further
comprises:
a descriptive coding of an error-handling module to receive the test
response signal and the expected test response signal and creates
a diagnostic signal indicating a location of any fault determined to
exist within said integrated circuits.
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40. The computer implemented hardware description coding of claim 39
wherein said descriptive coding of error handling module comprises:
descriptive coding of a serial shift register composed of flip-flops, which
are presettable from the serial-to-parallel data bus from the RAM
5 and said shift register is loaded by the PASS/FAIL signal from the
comparator, and whereby the serial output from the shift register
transfers the data for diagnosis.
41. The computer implemented hardware description coding of claim 33
10 wherein said hardware description coding of said test pattern generation
and comparison apparatus requires the number of bits of the test stimulus
signal and the adjusting in time of the test stimulus signal as parameters
to automatically create the physical description of said test pattern
generation and comparison apparatus during an automatic physical
15 design of said integrated circuit for placement on said semiconductor
substrate.
42. The computer implemented hardware description coding of claim 29
wherein said functional integrated circuits are selected from a group of
20 functional integrated circuits consisting of logic circuits and memory array
circuits.

43. A data retention medium readable by a computer system containing a hardware description coding providing a description of a data retention medium to automatically create a physical description of said data retention medium during an automatic physical design of said integrated circuit for placement on said semiconductor substrate, whereby said hardware description coding comprises:

a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits, whereby said test stimulus signal has a plurality of bits; and

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said test stimulus signals and to adjust in time the relationship of said test stimulus signals as required by said functional integrated circuits.

44. The data retention medium of claim 43 further comprising:

20 a descriptive coding of a plurality of parallel-to-serial converters wherein each parallel-to-serial converter is connected to one of the plurality of latency buffers, to convert said test stimulus to a

serialized test stimulus signals to be scanned to a scan register of said functional integrated circuit.

45. The data retention medium of claim 43 wherein said a descriptive coding
5 of background and command decoder comprises:

descriptive coding of decode logic which decodes a high level command bus for activating RAM control signals, and whereby the decode logic also controls the transfer of the background pattern of expected results to the error control module.

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46. The data retention medium of claim 43 wherein said a descriptive coding
of latency buffer comprises

a descriptive coding of a plurality of serially connected flip-flop circuits, whereby a first flip-flop circuit of said plurality of serially connected flip-flop circuits has a data input connected to said background and command decoder to receive one bit of said test stimulus signal and an output connected to a subsequent flip-flop circuit of the serially connected flip-flop circuits, whereby each subsequent flip circuit of the serially connected flip-flop circuits has an output connected to the input of a following flip-flop circuit of said plurality of serially connected flip-flop circuits, and whereby a last flip-flop circuit has an input connected to an output of a previous flip-flop

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circuit and an output containing a delayed bit of said test stimulus signal.

47. The data retention medium of claim 46 whereby the adjusting in time of
5 the test stimulus signals is determined by a number of flip-flop circuits in
the plurality of serially connected flip-flop circuits and the number of
latency buffers of the plurality of latency buffers is determined by a
number of bits in the test stimulus signals.

- 10 48. The data retention medium of claim 47 wherein the number of flip-flop
circuits is determined by the formula:

$$N = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

15 λ is the adjusting in time, and

ϕ is the period of the test access clocking
signal.

49. The data retention medium of claim 44 wherein the parallel-to-serial circuit
20 comprises:
a descriptive coding of a first plurality of flip-flops whereby each flip-
flop has a data input to receive one of a first portion of bits of said

test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the test stimulus signal;

a descriptive coding of a first plurality of multiplexor circuits whereby each multiplexor circuit has a first input to receive one of a remaining portion of bits of said test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

5 a descriptive coding of a second plurality of flip-flops, whereby each flip-flop of said plurality of flip-flops has a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the output of one of the first plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and

10 a descriptive coding of a second plurality of multiplexor circuits whereby each multiplexor circuit has a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select

15 input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

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50. The data retention medium of claim 43 further comprising:
a descriptive coding of a test response comparison circuit connected to
said background and control decoder to receive an expected test
5 response signal providing a correct response expected from said
integrated circuits in response to said test stimulus signals, and
connected to said integrated circuit to receive a test response
signal that is the response of the integrated circuit to said test
stimulus signal.
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51. The data retention medium of claim 50 wherein the descriptive coding of
the test response comparison circuit comprises:
a descriptive coding of a comparator circuit to receive the test
response signal and the expected test response signal, compare
15 said test response signal to said expected test response signal and
produce a test results signal indicating functioning of said
integrated circuits.
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52. The data retention medium of claim 51 wherein said descriptive coding of
comparator circuit comprises:
descriptive coding of an exclusive OR and OR logic tree which
compares the RAM data output from the serial-to-parallel converter
to an expected data output pattern from the background data.

53. The data retention medium of claim 50 wherein said descriptive coding of
test response comparison circuit further comprises:
5 a descriptive coding of an error-handling module to receive the test
 response signal and the expected test response signal and creates
 a diagnostic signal indicating a location of any fault determined to
 exist within said integrated circuits.
54. The data retention medium of claim 53 wherein said descriptive coding of
error handling module comprises:
10 descriptive coding of a serial shift register composed of flip-flops, which
 are presettable from the serial-to-parallel data bus from the RAM
 and said shift register is loaded by the PASS/FAIL signal from the
 comparator, and whereby the serial output from the shift register
 transfers the data for diagnosis.
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55. The data retention medium of claim 46 wherein said hardware description
coding of said test pattern generation and comparison apparatus requires
the number of bits of the test stimulus signal and the adjusting in time of
20 the test stimulus signal as parameters to automatically create the physical
 description of said test pattern generation and comparison apparatus
 during an automatic physical design of said integrated circuit for
 placement on said semiconductor substrate.

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56. The data retention medium of claim 43 wherein said functional integrated circuits are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

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57. A method for generation of test patterns to be communicated to integrated circuits and comparison of test response patterns communicated from said integrated circuit to verify function of said integrated circuits, comprising the steps of:

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receiving a test pattern command indicating which tests are to be performed communicated to said integrated circuit;
receiving a background pattern code indicating a pattern of test stimulus signals to be communicated to said integrated circuit;
decoding said test pattern command and said background pattern code to create said test stimulus signals;
adjusting a timing relation of said test stimulus signals to provide correct timing relationships for said test stimulus signals; and
communicating said test stimulus signals to said integrated circuit.

- 20 58. The method of claim 57 further comprising the step of:

converting said test stimulus signals to a serial test stimulus signal;

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59. The method of claim 58 wherein communicating the test stimulus signals comprises the step of:
- scanning said serial test stimulus signal to a scan register of said integrated circuit.
60. The method of claim 58 wherein converting said test stimulus signals is accomplished in a parallel-to-parallel converter comprising:
- a first plurality of flip-flops whereby each flip-flop has a data input to receive one of a first portion of bits of said test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the test stimulus signal;
- a first plurality of multiplexor circuits whereby each multiplexor circuit has a first input to receive one of a remaining portion of bits of said test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;
- a second plurality of flip-flops, whereby each flip-flop of said plurality of flip-flops has a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the output of one of the first

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plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and
a second plurality of multiplexor circuits whereby each multiplexor circuit has a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

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61. The method of claim 57 wherein adjusting the timing relationship of said test stimulus signals is accomplished in a latency buffer comprising:
15 a plurality of serially connected flip-flop circuits, whereby a first flip-flop circuit of said plurality of serially connected flip-flop circuits has a data input connected to said background and command decoder to receive one bit of said test stimulus signal and an output connected to a subsequent flip-flop circuit of the serially connected flip-flop circuits, whereby each subsequent flip circuit of the serially connected flip-flop circuits has an output connected to the input of a following flip-flop circuit of said plurality of serially connected flip-flop circuits, and whereby a last flip-flop circuit has an input
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connected to an output of a previous flip-flop circuit and an output containing a delayed bit of said test stimulus signal.

62. The method of claim 57 further comprising the steps of:

- 5 creating an expected test response signal from said test pattern command and said background pattern code;
- receiving the test response signals from the integrated circuit in response to said test stimulus signal;
- comparing said test response signal to said expected test response signal;
- 10 if said test response signal and expected test response signal indicate said integrated circuit is functioning, communicating a favorable test signal; and
- if said test response signal and expected test response signal indicate said integrated circuit is not functioning, communicating an unfavorable test signal.
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63. The method of claim 61 wherein said comparator is accomplished by a comparator comprising:

- 20 an exclusive OR and OR logic tree which compares the RAM dataoutput from the serial-to-parallel converter to an expected data output pattern from the background data.

64. The method of claim 57 further comprising the step of:
converting said test response signal to a parallel test response signal
for comparison with the expected test response signal.

5 65. The method of claim 64 wherein said converting is accomplished by a
serial-to-parallel conversion circuit comprising:
four flip-flops per serial input where the output of the first flip-flop
transfers to the second flip-flop and the third flip-flop whose output
is the second parallel bit and whereby the second flip-flop transfers
to the fourth flip-flop whose output is the first parallel output bit.

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66. The method of claim 64 further comprising the step of:
evaluating the comparison of the test response signal and the
expected test response signal to identify a fault location within said
integrated circuit if said test response signal and expected test
response signal indicate said integrated circuit is not functioning.

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67. The method of claim 66 where in said evaluating is accomplished in an
error handling module comprising:
20 a serial shift register composed of flip-flops, which are presettable from
the serial-to-parallel data bus from the RAM and said shift register
is loaded by the PASS/FAIL signal from the comparator, and

whereby the serial output from the shift register transfersthe data
for diagnosis.

68. The method of claim 57 wherein said functional integrated circuits are
5 selected from a group of integrated circuits consisting of logic circuits and
memory array circuits.

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